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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,819	06/27/2003	Rajesh Kota	NWISP046	8385

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EXAMINER	
NASH, LASHANYA RENEE	
ART UNIT	**PAPER NUMBER**
2153	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/607,819	KOTA ET AL.	
	Examiner	Art Unit	
	LaShanya R. Nash	2153	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/17/04, 11/30/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to the papers filed 30 June 2003. Claims 1-31 are presented for further consideration.

Claim Objections

Claim 23 is objected to because of the following informalities: improper grammar. Appropriate correction is required.

Examiner suggests replacing "plurality of processor" with "plurality of processors" in claim 23, line 3.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Pereira (US Patent 5,781,726), hereinafter referred to as Pereira.

Regarding claim 1, Pereira teaches:

- A computer system (Figure 5), comprising:
- A first cluster (Figure 5-item 203) including a first plurality of processors (Figure 5-items 204-205) and a first interconnection controller (Figure 5-item 200), the first

plurality of processors and the first interconnection controller in communication using a point-to-point architecture (column 2,lines 7-25; column 6, lines 11-19);

- A second cluster (Figure 5-item 206) including a second plurality of processors (Figure 5-items 207-210) and the second interconnection controller (Figure 5-item 202), the second plurality of processors and the second interconnection controller in communication using point-to-point architecture (column 2,lines 7-25; column 6, lines 11-19), wherein polling for a link from the first interconnection controller to the second interconnection controller (i.e. smart polling) can be enabled or disabled by configured the first interconnection controller (column 4,lnes 20-56; column 6, lines 20-49).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-9, 12-20 and 23-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pereira (US Patent 5,781,726) in view of Dervin et al. (US Patent 6,952,766).

Regarding claim 12, Pereira teaches:

- A method for introducing a cluster of processors (column 4, lines 20-42), the method comprising:
- Configuring a first interconnection controller (Figure 5-item 200), in a first cluster

(Figure 5-item 203) including a first plurality of processor in communication using a point-to-point architecture (column 2,lines 7-25; column 6, lines 11-19) to poll for the presence of a second interconnected controller (Figure 5-item 202), (i.e. smart polling; column 4,lnes 20-56; column 6, lines 20-49);

- A second interconnection controller in a second cluster (Figure 5-item 206) including a second plurality of processors (Figure 5-items 207-210) in communication using a point-to-point architecture (column 2,lines 7-25; column 6, lines 11-19);
- Establishing a link layer protocol on a connection between the first and second interconnection controllers (column 6,lines 20-29).

Pereira fails to teach the method asserting a reset signal. However, this would have been an obvious modification to the method as taught by Pereira for one of ordinary skill in the art at the time of the invention, as further evidenced by Dervin.

In an analogous art, Dervin teaches a method for automated node restart in clustered computing systems (abstract). Dervin further teaches asserting a reset (i.e. restart) signal in order to dynamically configure a cluster (column 5, lines 34-48; column 7, line 64-column 8, line 12; column 9, lines 7-18). One of ordinary skill in the art would have been so motivated to accordingly modify the method of Pereira so as to automate the process of detecting and initiating the restart of polled clusters thereby increasing availability and reducing operation intervention (Dervin; column 2, lines 58-62).

Regarding claim 23, Pereira teaches:

- A computer system (column 15, lines 1-55; Figure 9), comprising:

- A means for configuring a first interconnection controller (Figure 5-item 200), in a first cluster (Figure 5-item 203) including a first plurality of processor in communication using a point-to-point architecture (column 2,lines 7-25; column 6, lines 11-19) to poll for the presence of a second interconnected controller (Figure 5-item 202), (i.e. smart polling; column 4,lnes 20-56; column 6, lines 20-49);
- A means for a second interconnection controller in a second cluster (Figure 5-item 206) including a second plurality of processors (Figure 5-items 207-210) in communication using a point-to-point architecture (column 2,lines 7-25; column 6, lines 11-19);
- Means for establishing a link layer protocol on a connection between the first and second interconnection controllers (column 6,lines 20-29).

Pereira fails to teach the system asserting a reset signal. However, this would have been an obvious modification to the method as taught by Pereira for one of ordinary skill in the art at the time of the invention, as further evidenced by Dervin.

In analogous art, Dervin teaches a system for automated node restart in clustered computing systems (abstract). Dervin further teaches asserting a reset (i.e. restart) signal in order to dynamically configure a cluster (column 5, lines 34-48; column 7, line 64-column 8, line 12; column 9, lines 7-18). One of ordinary skill in the art would have been so motivated to accordingly modify the system of Pereira so as to automate the process of detecting and initiating the restart of polled clusters thereby increasing availability and reducing operation intervention (Dervin; column 2, lines 58-62).

Regarding claim 5, Pereira and Griffin fail to teach the method including a reinitialization indicator to direct a controller to reinitialize the link. However, this would have been an obvious modification to the method as taught by Pereira and Griffin for one of ordinary skill in the art at the time of the invention, as further evidenced by Dervin.

In an analogous art, Dervin teaches a method for automated node restart in clustered computing systems (abstract). Dervin further teaches reinitialization indicator (i.e. restart) to direct a controller to reinitialize the link (column 5, lines 34-48; column 7, line 64-column 8, line 12; column 9, lines 7-18). One of ordinary skill in the art would have been so motivated to accordingly modify the system of Pereira and Griffin so as to automate the process of detecting and initiating the restart of polled clusters thereby increasing availability and reducing operation intervention (Dervin; column 2, lines 58-62).

Regarding claim 6, Dervin teaches the method wherein reinitialization comprises having a transmitter associated with the first interconnection controller send a training sequence to the second interconnection controller (column 8, line 61-column 9, line 18).

Regarding claim 7, Pereira teaches the method transmitting a training sequence when the polling active state is set, (column 8, lines 27-41).

Regarding claim 8, Pereira teaches transmitting a training sequence when the polling sleep state is set (column 11, lines 10-17).

Regarding claim 9, Dervin teaches wherein reinitialization comprises having a transmitter associated with the first interconnection controller send an initialization sequence to the second interconnection controller (column 8, line 61-column 9, line 18).

Regarding claim 13 and 24, Pereira teaches wherein polling is performed continuously (column 6, lines 29-35).

Regarding claims 14 and 25, Pereira teaches the method wherein the first interconnection controller includes a physical layer enable indicator, (column 6,lines 20-30).

Regarding claims 15 and 26, Pereira teaches the method wherein the first interconnection controller includes a fence indicator configurable to prevent the transmission of logical packets between the first interconnection controller and the second interconnection controller (column 6, lines 43-49).

Regarding claims 16 and 27, Dervin further teaches reinitialization indicator (i.e. restart) to direct a controller to reinitialize the link (column 5, lines 34-48; column 7, line 64-column 8, line 12; column 9, lines 7-18).

Regarding claims 17 and 28, Dervin teaches the method wherein reinitialization

comprises having a transmitter associated with the first interconnection controller send a training sequence to the second interconnection controller (column 8, line 61-column 9, line 18).

Regarding claims 18 and 29, Pereira teaches the method transmitting a training sequence when the polling active state is set, (column 8, lines 27-41).

Regarding claims 19 and 30, Pereira teaches transmitting a training sequence when the polling sleep state is set (column 11, lines 10-17).

Regarding claims 20 and 31, Dervin teaches wherein reinitialization comprises having a transmitter associated with the first interconnection controller send an initialization sequence to the second interconnection controller (column 8, line 61-column 9, line 18).

Claims 2-4 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pereira (US Patent 5,781,726) in view of Griffin et al. (US Patent 6,889,263). Regarding claim 2, Pereira fails to teach wherein the first clusters of processors and the second cluster of processors share a single virtual address space. However, this would have been an obvious modification to the method as taught by Pereira for one of ordinary skill in the art at the time of the invention, as further evidenced by Griffin.

In an analogous art, Griffin teaches a method for changing cluster configuration (abstract). Griffin further teaches a first cluster of processors and the second cluster of processors share a single virtual address space (i.e. virtual address ranges; column 7,

lines 35-47; column 12, lines 1-22). One of ordinary skill in the art would have been motivated to accordingly modify the method of Pereira so as to manage a recover cluster resources, particularly virtual address space (Griffin; column 2, lines 15-24).

Regarding claim 3, Pereira teaches the method wherein the first interconnection controller includes a physical layer enable indicator, (column 6,lines 20-30).

Regarding claim 4, Pereira teaches the method wherein the first interconnection controller includes a fence indicator configurable to prevent the transmission of logical packets between the first interconnection controller and the second interconnection controller (column 6, lines 43-49).

Regarding claim 10, Pereira fails to teach the method wherein the first interconnection controller includes a plurality of cluster ID indicators operable to hold values identifying remote clusters of processors. However, this would have been an obvious modification to the method as taught by Pereira for one of ordinary skill in the art at the time of the invention, as further evidenced by Griffin.

In an analogous art, Griffin teaches a method for changing cluster configuration (abstract). Griffin further teaches the method wherein the first interconnection controller includes a plurality of cluster ID indicators operable to hold values identifying remote clusters of processors (column 7, lines 35-47). One of ordinary skill in the art would have been motivated to accordingly modify the method of Pereira so as to manage a

recover cluster resources, particularly virtual address space (Griffin; column 2, lines 15-24).

Regarding claim 11, Pereira fails to teach the method wherein the first interconnection controller includes configuration space registers comprising physical layer enable, fence, reinitialization, and cluster ID bits. However, this would have been an obvious modification to the method as taught by Pereira for one of ordinary skill in the art at the time of the invention, as further evidenced by Griffin.

In an analogous art, Griffin teaches a method for changing cluster configuration (abstract). Griffin further teaches the method wherein the first interconnection controller includes configuration space registers comprising physical layer enable, fence, reinitialization, and cluster ID bits (column 7, lines 35-47). One of ordinary skill in the art would have been motivated to accordingly modify the method of Pereira so as to manage a recover cluster resources, particularly virtual address space (Griffin; column 2, lines 15-24).

Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pereira in view of Dervin, as applied to claim 12 above, and further in view of Griffin et al. (US Patent 6,889,263).

Regarding claims 21 and 22, Pereira and Dervin fail to teach wherein the first interconnection controller includes a plurality of cluster ID indicators operable to hold values identifying remote clusters of processors [claim 21]; and wherein the first

interconnection controller includes configuration space registers comprising physical layer enable, fence, reinitialization, and cluster ID bits [claim 22]. However, this would have been an obvious modification to the method as taught by Pereira and Dervin for one of ordinary skill in the art at the time of the invention, as further evidenced by Griffin.

In an analogous art, Griffin teaches a method for changing cluster configuration (abstract). Griffin further teaches the method wherein the first interconnection controller includes a plurality of cluster ID indicators operable to hold values identifying remote clusters of processors (column 7, lines 35-47); and wherein the first interconnection controller includes configuration space registers comprising physical layer enable, fence, reinitialization, and cluster ID bits (column 7, lines 35-47). One of ordinary skill in the art would have been motivated to accordingly modify the method of Pereira and Dervin so as to manage and recover cluster resources (Griffin; column 2, lines 15-24).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LaShanya R. Nash whose telephone number is (571)272-3957. The examiner can normally be reached on 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glenton Burgess can be reached on (571) 272-3949. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LaShanya Nash
AU 2153
February 8, 2007

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